

32-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

| Device | Package Options | | | |
|--------|--|--|----------------------------------|---------|
| | 44 J-Lead Quad Ceramic Chip Carrier | 44 J-Lead Quad Plastic Chip Carrier | 44 Lead Quad Plastic Gullwing | Die |
| HV5122 | HV5122DJ | HV5122PJ | HV5122PG | HV5122X |
| HV5222 | HV5222DJ | HV5222PJ | HV5222PG | HV5222X |

Features

- Processed with HVCMOS® technology
- Output voltages to 225V using a ramped supply voltage
- Sink current minimum 100mA
- Shift register speed 8MHz
- Strobe and enable inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- 44-lead ceramic surface mount package
- Hi-Rel processing available

Absolute Maximum Ratings¹

| | | |
|--|--------------------------|----------------|
| Supply voltage, V_{DD} | -0.5V to +15V | |
| Output voltage, V_{PP} | -0.5V to +250V | |
| Logic input levels | -0.5V to $V_{DD} + 0.5V$ | |
| Ground current ² | 1.5A | |
| Continuous total power dissipation ³ | Plastic | 1200mW |
| | Ceramic | 1500mW |
| Operating temperature range | Plastic | -40°C to +85°C |
| | Ceramic | -55 to +125°C |
| Storage temperature range | -65°C to +150°C | |
| Lead temperature 1.6mm (1/16 inch) from case for 10 seconds | 260°C | |

Notes:

1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.

12/13/01

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General Description

The HV51 and HV52 are low voltage serial to high voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register and control logic to perform the Output Enable and All-ON functions. Data is shifted through the shift register on the high to low transition of the clock. The HV51 shifts in the counterclockwise direction when viewed from the top of the package and the HV52 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE (Output Enable) or the STR (Strobe) inputs.

The HV51 and HV52 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or which limit the current through each output.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|-----------------------------------|------------------------|-----|------|---------------|---|
| I_{DD} | V_{DD} supply current | | | 15 | mA | $f_{CLK} = 8\text{MHz}$ $F_{DATA} = 4\text{MHz}$ |
| I_{DDQ} | Quiescent V_{DD} supply current | | | 100 | μA | All $V_{IN} = 0\text{V}$ |
| $I_{O(OFF)}$ | Off state output current | | | 10 | μA | All outputs high All SWS parallel |
| I_{IH} | High-level logic input current | | | 1 | μA | $V_{IH} = 12\text{V}$ |
| I_{IL} | Low-level logic input current | | | -1 | μA | $V_{IL} = 0\text{V}$ |
| V_{OH} | High-level output data out | $V_{DD} - 1.0\text{V}$ | | | V | $I_{Dout} = -100\mu\text{A}$ |
| V_{OL} | Low-level output voltage | HV_{OUT} | | 15.0 | V | $I_{HVout} = +100\text{mA}$ |
| | | Data out | | 1.0 | V | $I_{Dout} = +100\mu\text{A}$ |
| V_{OC} | HV_{OUT} Clamp Voltage | | | -1.5 | V | $I_{OL} = -100\text{mA}$ |

AC Characteristics ($V_{DD} = 12\text{V}$, $T_C = 25^\circ\text{C}$)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|--------------------------------------|-----|-----|-----|-------|---------------------------------|
| f_{CLK} | Clock frequency | | | 8 | MHz | |
| t_W | Clock width high or low | 62 | | | ns | |
| t_{SU} | Data set-up time before clock falls | 25 | | | ns | |
| t_H | Data hold time after clock falls | 10 | | | ns | |
| t_{ON} | Turn ON time, HV_{OUT} from strobe | | | 500 | ns | $R_L = 2\text{K}\Omega$ to 200V |
| t_{DHL} | Delay time clock to data high to low | | | 100 | ns | $C_L = 15\text{pF}$ |
| t_{DLH} | Delay time clock to data low to high | | | 100 | ns | $C_L = 15\text{pF}$ |

Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units | |
|------------|--------------------------------|----------------------|-----|----------|-------|------------------|
| V_{DD} | Logic supply voltage | 10.8 | 12 | 13.2 | V | |
| HV_{OUT} | High voltage output | -0.3 | | 225 | V | |
| V_{IH} | High-level input voltage | $V_{DD} - 2\text{V}$ | | V_{DD} | V | |
| V_{IL} | Low-level input voltage | 0 | | 2.0 | V | |
| f_{CLK} | Clock frequency | | | 8 | MHz | |
| T_A | Operating free-air temperature | Plastic | | -40 | +85 | $^\circ\text{C}$ |
| | | Ceramic | | -55 | +125 | $^\circ\text{C}$ |

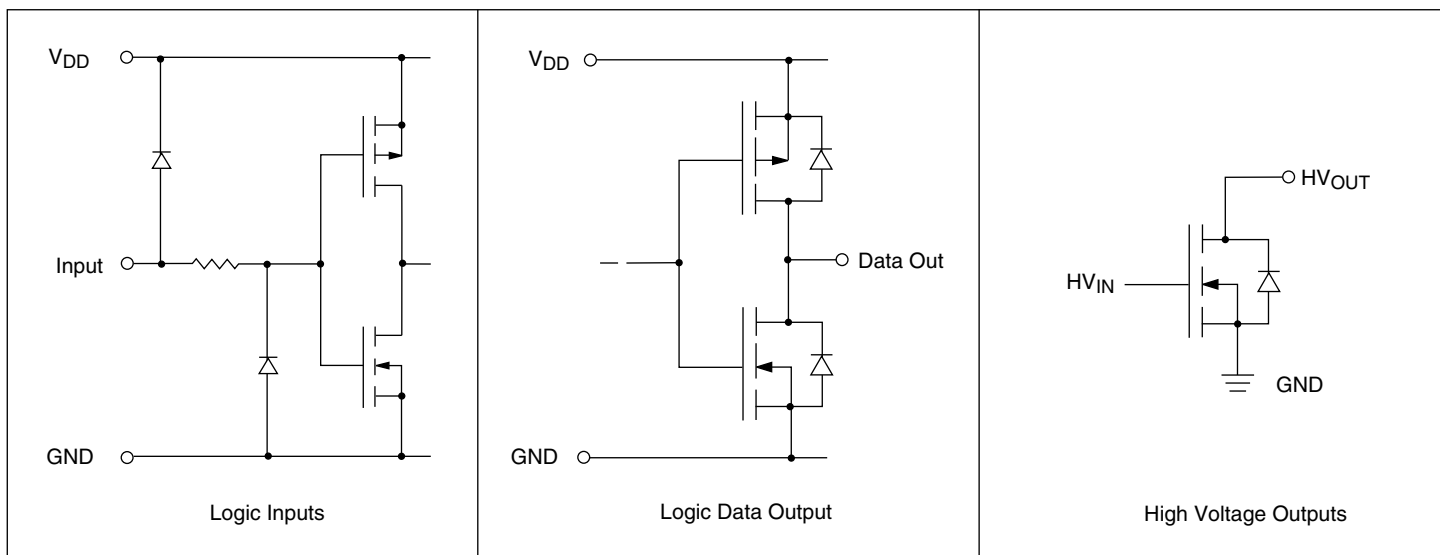
Notes:

Power-up sequence should be the following:

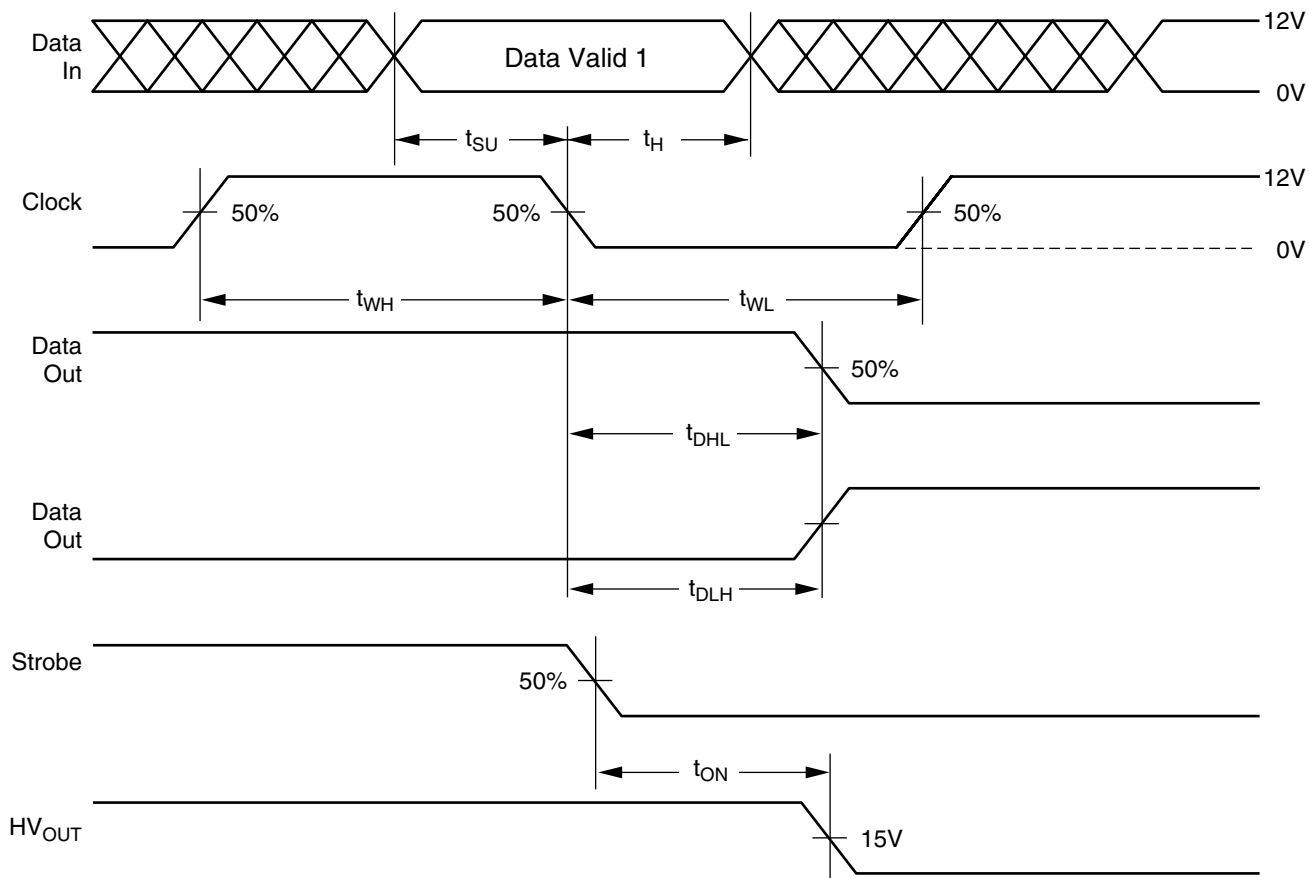
1. Connect ground.
2. Apply V_{DD} .
3. Connect all inputs to a known state.

Power-down sequence should be the reverse of the above.

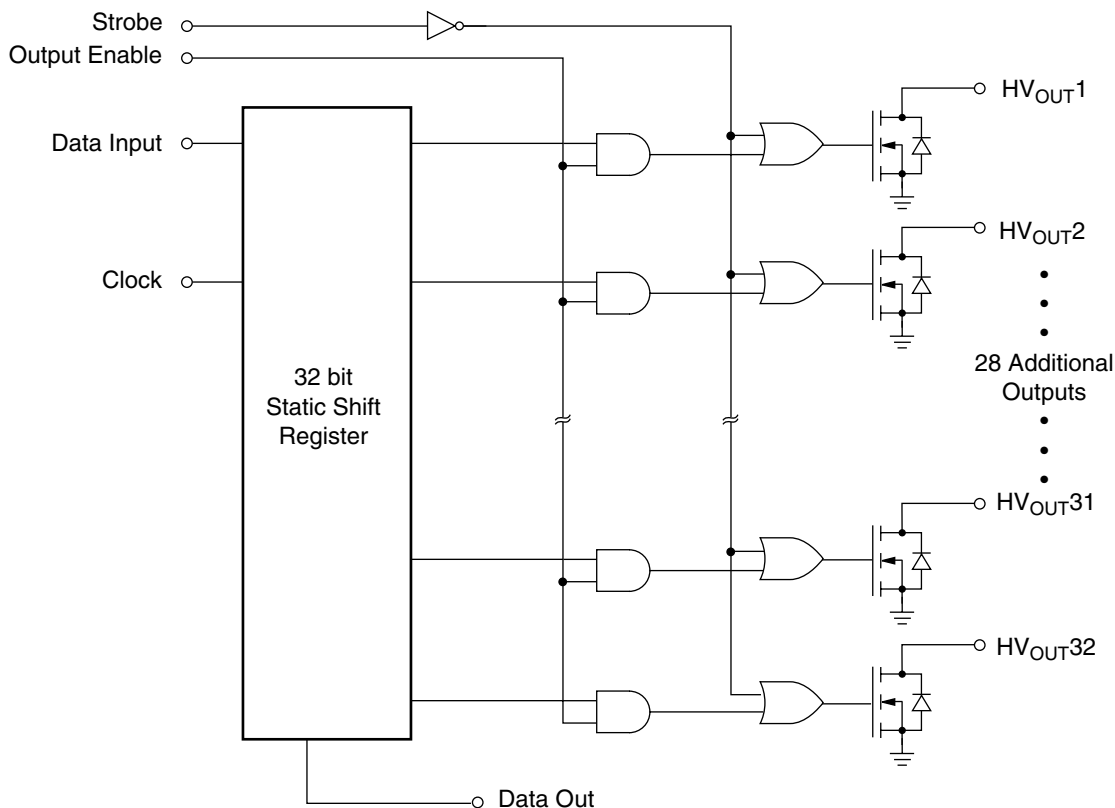
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

| Function | Inputs | | | | Outputs | | | |
|---------------|---------|--------|----|--------|-----------------------|------------------------|-----------|---------------|
| | Data In | CLK | OE | Strobe | Shift Reg 1 2...32 | HV Outputs 1 2...32 | | Data Out * |
| All on | X | X | X | L | * *...* | ON | ON...ON | * |
| All off | X | X | L | H | * *...* | OFF | OFF...OFF | * |
| Load S/R | H or L | ↓ | L | H | H or L *...* | OFF | OFF...OFF | |
| Output enable | X | H or L | H | H | H or L *...* | ON or OFF | *...* | * |

Notes:

X = Don't care

* = Dependent on previous stage's state before the last CLK : High to low transition.

↓ = High to low transition

H = High level

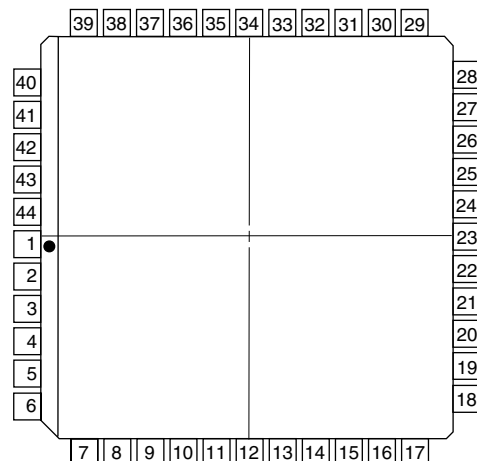
L = Low level

Pin Configurations

Package Outline

HV51 44 Pin J-Lead Package

| Pin | Function | Pin | Function |
|-----|----------------------|-----|----------------------|
| 1 | HV _{OUT} 16 | 23 | Output Enable |
| 2 | HV _{OUT} 17 | 24 | Clock |
| 3 | HV _{OUT} 18 | 25 | GND |
| 4 | HV _{OUT} 19 | 26 | V _{DD} |
| 5 | HV _{OUT} 20 | 27 | Strobe |
| 6 | HV _{OUT} 21 | 28 | Data In |
| 7 | HV _{OUT} 22 | 29 | N/C |
| 8 | HV _{OUT} 23 | 30 | HV _{OUT} 1 |
| 9 | HV _{OUT} 24 | 31 | HV _{OUT} 2 |
| 10 | HV _{OUT} 25 | 32 | HV _{OUT} 3 |
| 11 | HV _{OUT} 26 | 33 | HV _{OUT} 4 |
| 12 | HV _{OUT} 27 | 34 | HV _{OUT} 5 |
| 13 | HV _{OUT} 28 | 35 | HV _{OUT} 6 |
| 14 | HV _{OUT} 29 | 36 | HV _{OUT} 7 |
| 15 | HV _{OUT} 30 | 37 | HV _{OUT} 8 |
| 16 | HV _{OUT} 31 | 38 | HV _{OUT} 9 |
| 17 | HV _{OUT} 32 | 39 | HV _{OUT} 10 |
| 18 | Data Out | 40 | HV _{OUT} 11 |
| 19 | N/C | 41 | HV _{OUT} 12 |
| 20 | N/C | 42 | HV _{OUT} 13 |
| 21 | N/C | 43 | HV _{OUT} 14 |
| 22 | N/C | 44 | HV _{OUT} 15 |



top view
44-pin J-Lead Package

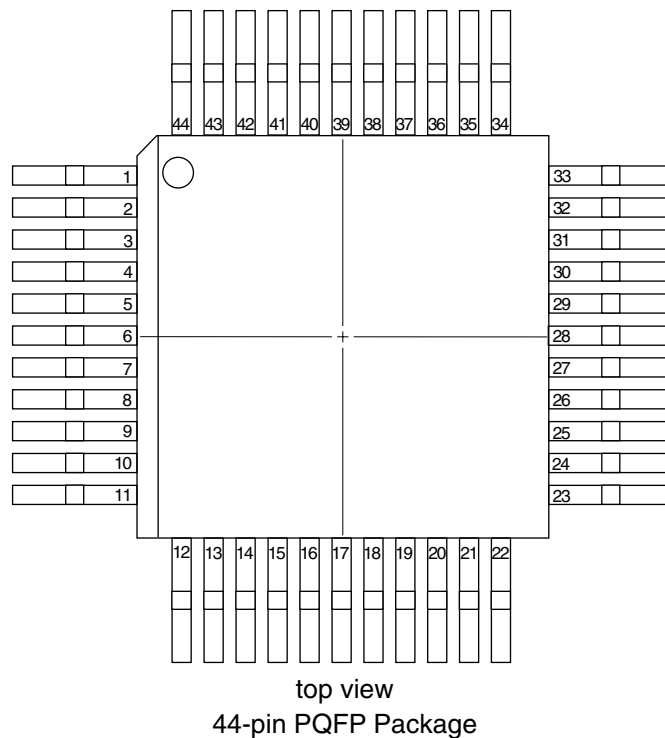
Pin Configurations

HV51

44-Pin Quad Plastic Package

| Pin | Function | Pin | Function |
|-----|----------------------|-----|----------------------|
| 1 | HV _{OUT} 11 | 23 | Data Out |
| 2 | HV _{OUT} 12 | 24 | N/C |
| 3 | HV _{OUT} 13 | 25 | N/C |
| 4 | HV _{OUT} 14 | 26 | N/C |
| 5 | HV _{OUT} 15 | 27 | N/C |
| 6 | HV _{OUT} 16 | 28 | Output Enable |
| 7 | HV _{OUT} 17 | 29 | CLK |
| 8 | HV _{OUT} 18 | 30 | GND |
| 9 | HV _{OUT} 19 | 31 | V _{DD} |
| 10 | HV _{OUT} 20 | 32 | Strobe |
| 11 | HV _{OUT} 21 | 33 | Data In |
| 12 | HV _{OUT} 22 | 34 | N/C |
| 13 | HV _{OUT} 23 | 35 | HV _{OUT} 1 |
| 14 | HV _{OUT} 24 | 36 | HV _{OUT} 2 |
| 15 | HV _{OUT} 25 | 37 | HV _{OUT} 3 |
| 16 | HV _{OUT} 26 | 38 | HV _{OUT} 4 |
| 17 | HV _{OUT} 27 | 39 | HV _{OUT} 5 |
| 18 | HV _{OUT} 28 | 40 | HV _{OUT} 6 |
| 19 | HV _{OUT} 29 | 41 | HV _{OUT} 7 |
| 20 | HV _{OUT} 30 | 42 | HV _{OUT} 8 |
| 21 | HV _{OUT} 31 | 43 | HV _{OUT} 9 |
| 22 | HV _{OUT} 32 | 44 | HV _{OUT} 10 |

Package Outline



HV52

44-Pin Quad Plastic Package

| Pin | Function | Pin | Function |
|-----|----------------------|-----|----------------------|
| 1 | HV _{OUT} 22 | 23 | Data Out |
| 2 | HV _{OUT} 21 | 24 | N/C |
| 3 | HV _{OUT} 20 | 25 | N/C |
| 4 | HV _{OUT} 19 | 26 | N/C |
| 5 | HV _{OUT} 18 | 27 | N/C |
| 6 | HV _{OUT} 17 | 28 | Output Enable |
| 7 | HV _{OUT} 16 | 29 | CLK |
| 8 | HV _{OUT} 15 | 30 | GND |
| 9 | HV _{OUT} 14 | 31 | V _{DD} |
| 10 | HV _{OUT} 13 | 32 | Strobe |
| 11 | HV _{OUT} 12 | 33 | Data In |
| 12 | HV _{OUT} 11 | 34 | N/C |
| 13 | HV _{OUT} 10 | 35 | HV _{OUT} 32 |
| 14 | HV _{OUT} 9 | 36 | HV _{OUT} 31 |
| 15 | HV _{OUT} 8 | 37 | HV _{OUT} 30 |
| 16 | HV _{OUT} 7 | 38 | HV _{OUT} 29 |
| 17 | HV _{OUT} 6 | 39 | HV _{OUT} 28 |
| 18 | HV _{OUT} 5 | 40 | HV _{OUT} 27 |
| 19 | HV _{OUT} 4 | 41 | HV _{OUT} 26 |
| 20 | HV _{OUT} 3 | 42 | HV _{OUT} 25 |
| 21 | HV _{OUT} 2 | 43 | HV _{OUT} 24 |
| 22 | HV _{OUT} 1 | 44 | HV _{OUT} 23 |